

  
**Building Resilience to Climate Related Hazards Project**  
**Supply, Delivery and Installation of Equipment for ICT Infrastructure and Management**  
 (Contract ID No: PPCR/DHM/G/NCB-30)

**Clarification -3**

We received the following Clarification request through pre-bid meeting, official letter and email from the Consulting Firms. Our response is as follows:

| Query No | Reference to the Bid Document   | Description of Queries   | DHM /BRCH Clarification  |
|----------|---|--|--|
| 1        | Section V Schedule of Requirements, Chapter 3. Technical specification, Sub-Heading 3.7.1 The mandatory requirements for the storage system, Sub-Heading-Disk Capacity " 24x600GB 15k SAS, 24x3TB NL 7.2k SAS, should include hot-spare configuration as per vendor best-practice (Page-70) | <p>As you have clarified as Two different storage groups, both of them need hot-space configuration as per vendor best-practice.</p> <p>Please make us clear; does this means there is a requirement of two hardware in which one hardware should have 24x600GB 15k SAS and other hardware should have 24x3TB NL 7.2k SAS, should include hot-spare configuration as per vendor best-practice.</p> <p>OR</p> <p>Single storage with 48 Hard disks supporting 24x3TB NL 7.2k SAS and 24x600GB 15k SAS</p> | Single storage with 48 Hard disks supporting 24x3TB NL 7.2k SAS and 24x600GB 15k SAS. Both storage groups should have own hot-spare configuration as per vendor best-practice. |
| 2        |   | <p>We are going to participating this project with EMC storage, However EMC do not have 3TB 7.2K RPM SAS disk. So we decided to give higher specification that is 4TB 7.2K RPM instead of 3TB. Hope this is acceptable for your project.</p> <p>We have little confusion of Cache memory is it total 16GB in two controller (8GB + 8GB) or Per controller 16GB (32GB total in dual controller). Request you to make us clear on this.</p>  | The 8GB per controller should be enough, but if the price difference is not significant, take 16GB per controller. What is important is that the cache is battery-backed.      |

*Sana*